

Claims

- [c1] 1. A method for fabricating interconnects, comprising:
 - forming a conducting line on a first dielectric layer;
 - forming a first liner layer on the surfaces of said first dielectric layer and said conducting line;
 - forming a second liner layer on said first liner, said dielectric layer having an etching rate;
 - forming a second dielectric layer on said second liner, said second dielectric layer having an etching rate higher than said etching rate of said second liner; and
 - patterning said second dielectric layer to form a contact window opening through said second liner layer and said first liner layer to expose the surface of said conducting line.
- [c2] 2. The method of claim 1, wherein said conducting line is formed by stacking a first barrier layer, an Al-dominated metal layer, and a second barrier layer.
- [c3] 3. The method of claim 2, wherein each of said first barrier and second barrier layers is a TiN layer or a stacked layer comprising a TiN layer and a Ti layer.
- [c4] 4. The method of claim 1, wherein said step of forming

said first liner layer includes performing a high-density plasma chemical vapor deposition (HDPCVD) process.

- [c5] 5.The method of claim 1, wherein materials of said first liner and said second dielectric layer are same.
- [c6] 6.The method of claim 1, wherein an etch selectivity ratio of said second dielectric layer to said second liner is between 50 and 70.
- [c7] 7.The method of claim 1, wherein said second dielectric layer includes silicon oxide.
- [c8] 8.The method of claim 1, wherein said second liner is SiN_x or SiON .
- [c9] 9.The method of claim 1, wherein before said step of forming said conducting line, the method further comprises forming a contact window in said first dielectric layer, and said contact window being electrically connected to said conducting line.
- [c10] 10.The method of claim 1, wherein before said step of forming said contact window opening, the method further comprises filling a conducting layer into said contact window opening.
- [c11] 11. An interconnect structure, comprising:
 - a first dielectric layer;

a conducting line disposed on said first dielectric layer;
a first liner layer disposed on surfaces of said first dielectric layer and said conducting line;
a second liner layer disposed on a surface of said first liner; and
a second dielectric layer covering said second liner, said second dielectric layer comprising a contact widow opening therein through said second liner layer and said first liner layer to expose the surface of said conducting line.

- [c12] 12. The interconnect structure of claim 11, wherein said conducting line is formed by stacking a first barrier layer, an Al-dominated metal layer, and a second barrier layer.
- [c13] 13. The interconnect structure of claim 12, wherein each of said first barrier and second barrier layers is a TiN layer or a stacked layer comprising a TiN layer and a Ti layer.
- [c14] 14. The interconnect structure of claim 11, wherein materials of said first liner layer and said second dielectric layer are the same.
- [c15] 15. The interconnect structure of claim 11, wherein an

etch selectivity ratio of said second dielectric layer to said second liner is between 50 and 70.

- [c16] 16.The interconnect structure of claim 11, wherein said second dielectric layer includes silicon oxide.
- [c17] 17.The interconnect structure of claim 11, wherein said second liner layer is SiN_x or SiON.
- [c18] 18.The interconnect structure of claim 11 further comprising a contact window in said first dielectric layer, said contact window being electrically connected to said conducting line.
- [c19] 19.The interconnect structure of claim 11, further comprising a conducting layer filled into said contact window opening.